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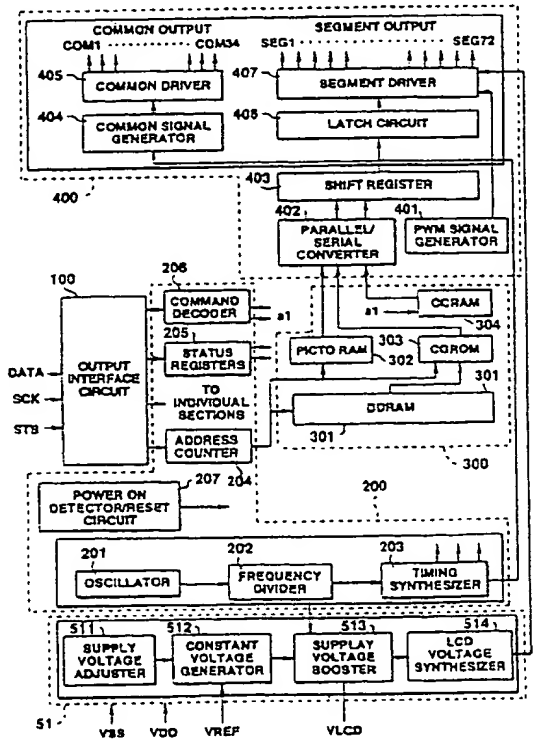
(54) Title: ELECTRICALLY CONTROLLED BIRIFRINGENCE LIQUID CRYSTAL DISPLAY HAVING MORE DISPLAY AREAS AND METHOD OF DRIVING THE SAME

(57) Abstract

An electrically controlled birifringence type liquid crystal display panel has a pictograph (picto) display area and character display areas. Character codes are stored in a DDRAM (301) and color attribute data indicating the display colors of characters are stored in a CCRAM (302), both in one-to-one association with the character display areas. Character patterns for character codes stored in the DDRAM (301) are read from a character generator (303), and, simultaneously color attribute data in the CCRAM (304) is read out. A segment driver (407) controls voltages to be applied to the liquid crystal display panel based on the character pattern and the color attribute data, for displaying the characters in arbitrary colors. Color attribute data which specifies the display color of each of pixels constituting a pictograph is set in a picto RAM (302). The color attribute data of the individual segments are read from the picto RAM (302) at the timing for displaying a pictograph, and the segment driver (407) controls voltages to be applied to the liquid crystal display panel in accordance with this color attribute data, for displaying pictograph on the pictograph display area.



light then passes the lower polarization plate 41, is reflected by the reflector 43, and travels in the opposite path to leave the LCD panel 3. The outgoing light is colored with the color according to the retardation of the retardation plate 42.

The display area of the LCD panel 3 will now be discussed.

The LCD panel 3 has 34 common electrodes 38 and 72 segment electrodes 36 as mentioned earlier, and has a plurality of pixels defined by the opposing portions of the common electrodes 38 and the segment electrodes 36.

As shown in Fig. 3, the upper area of a display area 3a of the LCD panel 3 constitutes a pictograph (hereinafter referred to as "picto") display area 3c, and the lower area constitutes a segment display area (character display areas) 3b.

The individual pixels of the segment display area 3b are shaped like dots. The segment display area 3b has a dot pattern of 72 dots x 32 dots by which it displays arbitrary characters (including numerals and symbols). The display positions and sizes of characters are fixed, and there are 4 lines by 12 digits of character display areas each having a size of 8 x 6 dots.

The individual pixels of the picto display area 3c are patterned in arbitrary shapes to form predetermined images. In Fig. 3, the display patterns are "Eng.", "Jap." and the frames surrounding the former two. Of the 72 segment electrodes 36, predetermined three segment electrodes 36

are patterned in those shapes. The first common electrode 38 faces the frame patterns and the second common electrode 38 faces the "Eng." and "Jap.".

The drive controller 5 performs the matrix driving of the entire common electrodes 38 and segment electrodes 36, i.e., the entire display area 3a, to display an image.

The drive controller 5 will now be described.

Fig. 4 presents a block diagram showing the overall circuit structure of the color LCD apparatus 1 according to this embodiment.

The drive controller 5 is connected between the LCD panel 3 and a display controller 10 which performs data processing to produce display data. The drive controller 5 produces an LC drive voltage (which will be discussed later) according to a display color in accordance with serial input data DATA, a serial interface shift clock signal SCK and a serial interface input enable signal STB, all input from the display controller 10. The drive controller 5 applies the LC drive voltage to the LCD panel 3 to display characters in multiple colors.

The drive controller 5 comprises a power supply section 51, an output interface circuit 100, a control section 200, a memory section 300 and an LCD driver 400, as shown in Fig. 4.

Fig. 5 is a block diagram showing the detailed structure of the drive controller 5.

As shown in Fig. 5, the power supply section 51 includes a supply voltage adjuster 511, a constant voltage

generator 512, a supply voltage booster 513 and an LCD voltage synthesizer 514.

The control section 200 includes an oscillator 201, a frequency divider 202, a timing synthesizer 203, an address counter 204, a plurality of status registers 205, a command decoder 206 and a power ON detector/reset circuit 207.

The memory section 300 includes a display data RAM (DDRAM) 301, a picto RAM 302, a character generator ROM (CGROM) 303 and a character color RAM (CCRAM) 304.

The LCD driver 400 includes a gradation PWM (Pulse Width Modulation) signal generator 401, a parallel/serial converter 402, a shift register 403, a common signal generator 404, a common driver 405, a latch circuit 406 and a segment driver 407.

A description will now be given of the power supply section 51.

The constant voltage generator 512 is comprised of a constant voltage source and generates a constant voltage from a supply voltage V_{DD}, a ground voltage V_{SS} and a reference voltage V_{REF}. The supply voltage adjuster 511 adjusts the value of the constant voltage which is generated by the constant voltage generator 512. The supply voltage booster 513 boosts the constant voltage generated by the constant voltage generator 512. The LCD voltage synthesizer 514 receives the supply voltage boosted by the supply voltage booster 513, combines a plurality of voltages needed to drive the segment electrodes, and supplies the resultant voltage to the segment driver 407.

The output interface circuit 100 converts the serial input data DATA, the serial interface shift clock signal SCK and the serial interface input enable signal STB, supplied from the display controller 10, to levels or data which can be processed in the drive controller 5, and sends the results to the individual sections in the drive controller 5.

The control section 200 will be discussed below. The oscillator 201 generates a reference oscillation signal from the serial interface shift clock signal SCK supplied from the display controller 10. The frequency divider 202 frequency-divides the reference oscillation signal from the oscillator 201 by a predetermined frequency-dividing ratio. The timing synthesizer 203 synthesizes acquires a timing signal to drive the common electrodes from the frequency-divided signal from the frequency divider 202, and supplies the timing signal to the common signal generator 404.

The address counter 204 counts the addresses of data to be displayed, stored in the DDRAM 301 and the picto RAM 302, based on the serial interface shift clock signal SCK supplied from the output interface circuit 100. The address counter 204 sends out the counted addresses to the DDRAM 301 and the picto RAM 302.

The status register group 205 comprises a plurality of registers for temporarily storing character data, color attribute data, display color specifying palette data and the like included in the serial input data DATA input from the output interface circuit 100.

The command decoder 206 decodes a command included in serial input data DATA from the output interface circuit 100 and controls the individual sections according to the decoded result.

The power ON detector/reset circuit 207 detects the power ON action of the color LCD apparatus 1 and resets the individual sections of the drive controller 5.

A description will now be given of the memory section 300.

The DDRAM 301 has a plurality of memory areas of 4 x 12 bits in association of the character display areas 3b of 4 lines by 12 digits, as shown in Fig. 6. Each memory area stores 8-bit character data (code data). The address of each memory area in the DDRAM 301 consists of six bits (upper two bits (DDH1 and DDH2) and lower two bits (DDL1 to DDL4). The memory addresses of the DDRAM 301 correspond to the character display positions of the character display areas 3b in a one-to-one relation. When a character "B" is to be displayed on the character display area 3b at the first line and the second column as shown in Fig. 3, for example, 8-bit character data (code) of the character "B" is stored at the upper address (DDH2, DDH1) = 01) and the lower address (DDL1-DDL4) = (1000) in the DDRAM 301.

The memory contents of the DDRAM 301 can be set and changed arbitrarily by the display controller 10 in accordance with the display contents.

Fig. 7 shows the memory structure of the picto RAM 302.

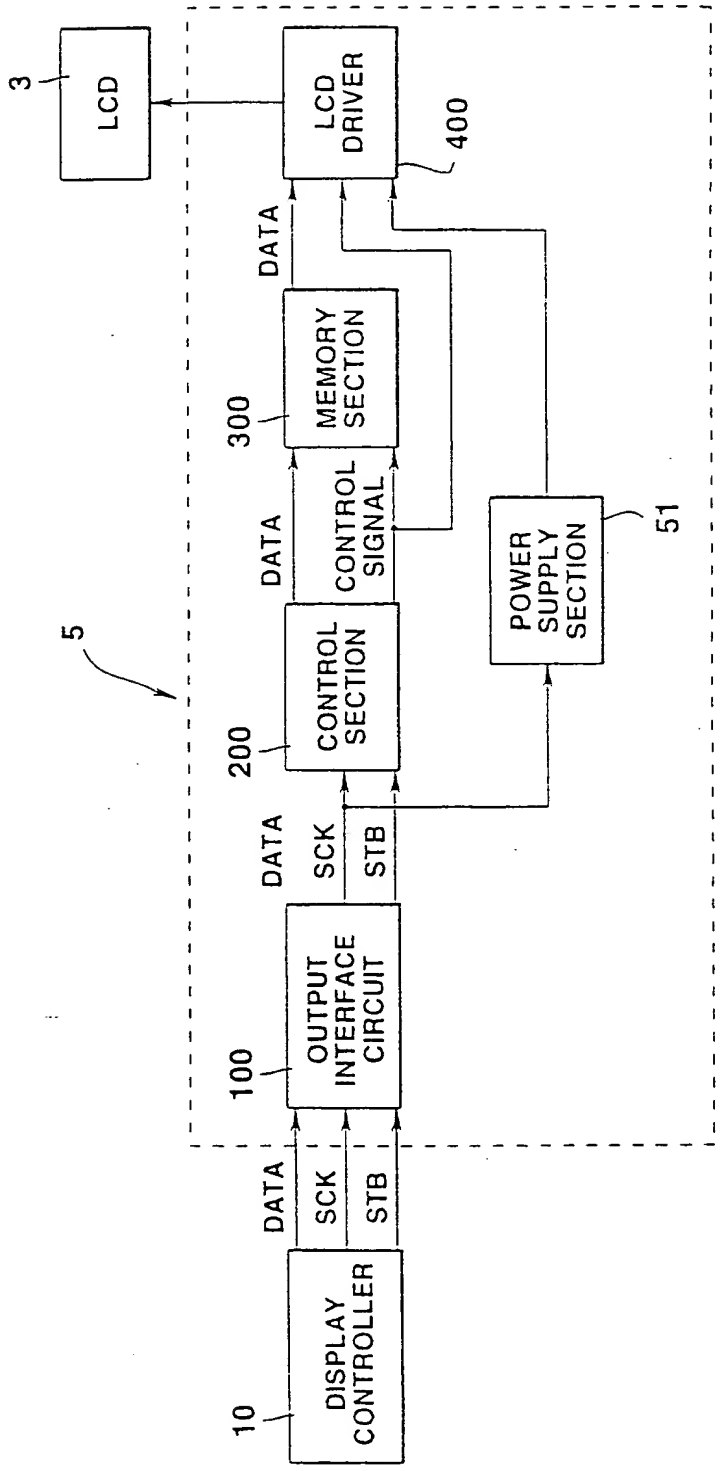

3
LCD
LCD DRIVER
400
DATA
MEMORY SECTION
300
DATA
CONTROL SIGNAL
POWER SUPPLY SECTION
51
5
CONTROL SECTION
200
DATA
SCK
STB
OUTPUT INTERFACE CIRCUIT
100
DATA
SCK
STB
DISPLAY CONTROLLER
10

FIG.4

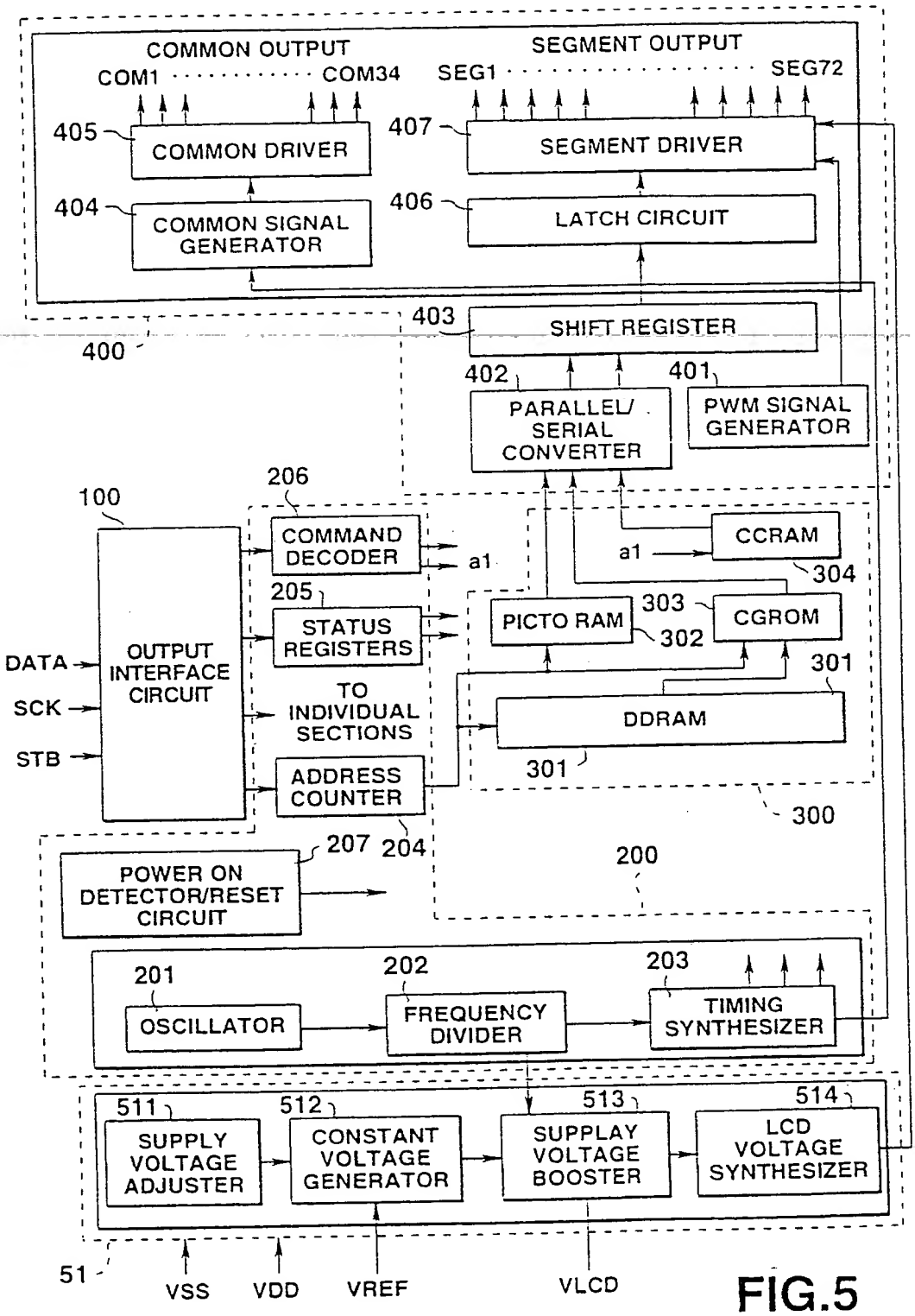

COMMON OUTPUT
COM1
COM34
SEGMENT OUTPUT
SEG1
SEG72
405
COMMON DRIVER
407
SEGMENT DRIVER
404
COMMON SIGNAL GENERATOR
406
LATCH CIRCUIT
400
403
SHIFT REGISTER
402
401
PARALLEL/ SERIAL CONVERTER
PWM SIGNAL GENERATOR
206
100
COMMAND DECODER
a1
a1
CCRAM
304
205
303
PICTO RAM
CGROM
302
DATA
OUTPUT INTERFACE CIRCUIT
STATUS REGISTERS
301
SCK
TO INDIVIDUAL SECTIONS
DDRAM
STB
ADDRESS COUNTER
301
300
207
204
200
POWER ON DETECTOR/RESET CIRCUIT
201
202
203
OSCILLATOR
FREQUENCY DIVIDER
TIMING SYNTHESIZER
511
512
513
514
SUPPLY VOLTAGE ADJUSTER
CONSTANT VOLTAGE GENERATOR
SUPPLAY VOLTAGE BOOSTER
LCD VOLTAGE SYNTHESIZER
51
VSS
VDD
VREF
VLCD

FIG.5